

What is claimed is:

1 1. A method of forming a bit line contact hole,
2 comprising:

3 providing a substrate having a transistor thereon,
4 wherein the transistor comprises a gate layer
5 covered by a first insulating layer, and a
6 doped region;

7 forming a polysilicon layer to conformally cover the
8 substrate and the transistor;

9 defining the polysilicon layer to form an inner
10 landing pad connecting with the doped region;

11 conformally forming a passivation layer on the inner
12 landing pad, the transistor, and the substrate;

13 forming a second insulating layer with a flat
14 surface on the passivation layer;

15 forming a contact hole in the second insulating
16 layer and the passivation layer to expose the
17 inner landing pad; and

18 filling a metal layer in the contact hole.

1 2. The method as claimed in claim 1, wherein the
2 thickness of the polysilicon layer is about 100~400Å.

1 3. The method as claimed in claim 1, wherein the
2 polysilicon layer is defined by wet etching.

1 4. The method as claimed in claim 3, wherein an
2 etching agent of etching polysilicon comprises an HF
3 solution.

1 5. The method as claimed in claim 4, wherein the
2 etching agent comprises NH_4F and HF of about 400~500:1.

1 6. The method as claimed in claim 1, the material
2 of the passivation layer comprises silicon nitride.

1 7. The method as claimed in claim 1, wherein the
2 thickness of the passivation layer is about 110~130Å.

1 8. The method as claimed in claim 1, wherein the
2 second insulating layer is a stacked layer comprising a
3 boro-phospho silicate glass (BPSG) layer and a
4 tetraethylorthosilicate (TEOS) layer.

1 9. The method as claimed in claim 8, wherein
2 formation of the BPSG comprises depositing a BPSG
3 material on the passivation layer and polishing the BPSG
4 material until the passivation layer is exposed.

1 10. The method as claimed in claim 8, wherein the
2 thickness of the BPSG layer is about 5900~7300Å, and the
3 thickness of the TEOS layer is about 3600~4400Å.

1 11. The method as claimed in claim 1, wherein the
2 material of the metal layer comprises tungsten (W).

1 12. A method of forming a bit line contact hole,
2 suitable for a substrate having a transistor thereon and
3 comprising a memory cell array area and a logic circuit
4 area, the transistor comprising a gate layer covered by a
5 first insulating layer and a doped region, comprising:

6 forming a polysilicon layer to conformally cover the
7 substrate and the transistor;

8 defining the polysilicon layer to form an inner
9 landing pad connecting with the doped region in
10 the memory cell array area;
11 conformally forming a passivation layer on the inner
12 landing pad, the transistor, and the substrate;
13 forming a second insulating layer with a flat
14 surface on the passivation layer;
15 forming a first contact hole, a second contact hole,
16 and a third contact hole in the second
17 insulating layer and the passivation layer,
18 wherein the first contact hole exposes the
19 surface of the inner landing pad in the memory
20 cell array area, the second contact hole
21 exposes the gate layer of the transistor in the
22 logic circuit area, and the third contact hole
23 exposes the doped region of the transistor in
24 the logic circuit area; and

25 filling a metal layer in the first contact hole, the
26 second contact hole, and the third contact hole.

1 13. The method as claimed in claim 12, wherein the
2 thickness of the polysilicon layer is about 100~400Å.

1 14. The method as claimed in claim 12, wherein the
2 polysilicon layer is defined by wet etching.

1 15. The method as claimed in claim 14, wherein an
2 etching agent of etching polysilicon comprises an HF
3 solution.

1 16. The method as claimed in claim 15, wherein the
2 etching agent comprises NH_4F and HF of about 400~500:1.

1 17. The method as claimed in claim 12, the material
2 of the passivation layer comprising silicon nitride.

1 18. The method as claimed in claim 12, wherein the
2 thickness of the passivation layer is about 110~130Å.

1 19. The method as claimed in claim 12, wherein the
2 second insulating layer is a stacked layer comprising a
3 boro-phospho silicate glass (BPSG) layer and a
4 tetraethylorthosilicate (TEOS) layer.

1 20. The method as claimed in claim 19, wherein
2 formation of the BPSG comprises depositing a BPSG
3 material on the passivation layer and polishing the BPSG
4 material until the passivation layer is exposed.

1 21. The method as claimed in claim 19, wherein the
2 thickness of the BPSG layer is about 5900~7300Å, and the
3 thickness of the TEOS layer is about 3600~4400Å.

1 22. The method as claimed in claim 12, wherein the
2 material of the metal layer comprises tungsten (W).

1 23. A structure for a bit line contact hole,
2 comprising:

3 a substrate;

4 a transistor, disposed on the substrate, comprising

5 a gate layer covered by a first insulating

6 layer and a doped region;

7 an inner landing pad, disposed on the doped region
8 and parts of the transistor, comprising a
9 polysilicon layer;
10 a passivation layer, disposed on the inner landing
11 pad, the transistor, and the substrate;
12 a second insulating layer, disposed on the
13 passivation layer, having a flat surface on the
14 passivation layer;
15 a contact plug, disposed on the second insulating
16 layer and the passivation, electrically
17 connecting with the inner landing pad; and
18 an interconnected landing pad, deposited on the
19 contact plug.

1 24. The structure as claimed in claim 23, wherein
2 thickness of the polysilicon of the inner landing pad is
3 about 100~400Å.

1 25. The structure as claimed in claim 23, wherein
2 the material of the passivation comprises silicon
3 nitride.

1 26. The structure as claimed in claim 25, wherein
2 thickness of the passivation is about 110~130Å.